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| 10/013,087 | 12/07/2001 | Hideyuki Andoh | 44471-267680 (13700) | 1427 |
| 23370 | 7590 | 04/20/2004 | EXAMINER | |
| JOHN S. PRATT, ESQ KILPATRICK STOCKTON, LLP 1100 PEACHTREE STREET SUITE 2800 ATLANTA, GA 30309 | | | SCHILLINGER, LAURA M | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2813 | |
| DATE MAILED: 04/20/2004 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/013,087

Applicant(s)

ANDOH, HIDEYUKI

Examiner

Laura M Schillinger

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9, 12 and 13 is/are pending in the application.
- 4a) Of the above claim(s) 12 and 13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

Claims 12-13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim.

Applicant timely traversed the restriction (election) requirement in Paper dated 1/23/04.

Applicant asserts that claims 12 and 13 have common limitations and there would be no undue hardship upon the Examiner. However such an argument is not persuasive because as described a separate search would be required to address the limitations claimed by the Applicant and the newly added claims contain various distinguishing features which constitute distinct species from the claims which were originally pending.

Claim Rejections - 35 USC § 112

Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the phrase "metallurgical contact" does not exist within the specification. More Specifically there is no disclosure within the specification of the last limitation of claim 1 which recites "a fourth semiconductor region having first and second inner surfaces in metallurgical contact with the first and second side boundary surfaces respectively when viewed in section" is not found to be supported by the Applicant's specification. Applicant

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has therefore added new matter into the claims which is not supported by the original specification as filed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Jambotkar ('857).

In reference to claim 1, Jambotkar teaches a device comprising:

A first semiconductor region of a first conductivity type, defined by an upper end surface and a side boundary surface connecting the upper and lower end surfaces when viewed in section (Fig.2A (16));

A second semiconductor region of the first conductivity type in metallurgical contact (s1) with the first semiconductor region at the lower end surface (Fig.2A (14));

A third semiconductor region of a second conductivity type metallurgical contact (B1) with the first semiconductor region at the upper end surface (Fig.2A (12)); and

A fourth semiconductor region having inner surface in metallurgical contact (W1) with the side boundary surface when viewed in section and an impurity concentration lower than the

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first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions (Fig.2A (10)).

In reference to claim 2, Jambotkar teaches wherein the fourth semiconductor region has a first type conductivity (Fig.2A (10)).

In reference to claim 3, Jambotkar teaches wherein outer surface of the fourth semiconductor region serves as a chip outer surface of the semiconductor device and the chip outer surface is substantially orthogonal with the lower end surface of the first semiconductor region.

In reference to claim 4, Jambotkar teaches wherein the fourth semiconductor region is made of a wafer cut from bulk crystal (Fig.2A (10) and Col.7, lines: 15-20).

In reference to claim 5, Jambotkar teaches further comprising a first main electrode layer is formed on a bottom surface of the second semiconductor region (Fig.2A (S1)).

In reference to claim 6, Jambotkar teaches wherein the first main electrode layer is contacted with the second semiconductor region, through a first concavity formed at the bottom surface of the second semiconductor region (Fig.3 (20')).

In reference to claim 7, Jambotkar teaches further comprising a first main electrode layer, a part of the first main electrode layer is buried in a via hole penetrating through the second

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semiconductor region, configured such that the buried part of the first main electrode layer contacts with the first semiconductor region (Fig.2A (S1)).

In reference to claim 8, Jambotkar teaches further comprising a second main electrode layer is formed on a top surface of the third semiconductor region (Fig.4A (G1)).

In reference to claim 9, Jambotkar teaches wherein the second main electrode layer is contacted with the first semiconductor regions, through a second concavity formed at the top surface of the third semiconductor region (Fig.3 (20')).

Response to Arguments

Applicant's arguments filed 7/10/03 have been fully considered but they are not persuasive.

The arguments state, "region 14 of Jambotkar does not metallurgically contact region 16 because region 14 is used as a source region while region 16 is used as the drain region of a field effect transistor (see Column 2, lines 2 1-24). Although region 14 electrically contacts region 16 through an electrical connection, such as surface wiring, the regions are not in metallurgical contact because the regions are not connected via region-to-region contact. Therefore, Jambotkar fails to disclose a second semiconductor region of the first conductivity type being in metallurgical contact with the first semiconductor region at the lower end surface of the first semiconductor region"

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The Examiner disagrees with the assertion that regions 14 and 16 do not have a metallurgical contact. Specifically, Col.2, lines: 48-55 discusses the power supplied to both electrodes D1 and S1 thereby forming a metal contact between the two regions. The arguments attempt to define "metallurgical contact" as being a "region to region contact", the examiner does not understand what a "region to region contact" means both terminologies are not described within the specification.

The arguments further assert that ('857) fails to teach "a fourth semiconductor region having first and second inner surfaces in metallurgical contact with the first and second side boundary surfaces respectively when viewed in section" however this limitation is not supported by the specification.

Lastly, the arguments assert that layer (10) is not located between regions (12 and 14). This is not persuasive because (10) has a center region located between regions 12 and 14.

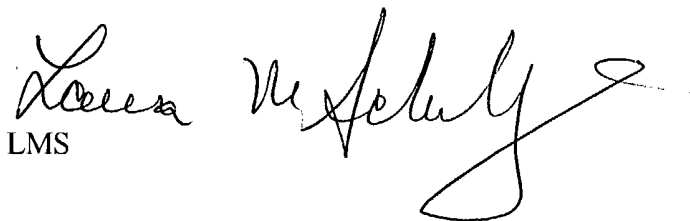
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


LMS

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